CLAIMS

What is claimed is:

1. A chip comprising:

a first port to provide a first received data signal and a first received strobe signal;

a second port to provide a second received data signal and a second received strobe signal;

circuitry to provide an internal clock signal with a fixed phase relationship to the first received strobe signal, wherein the second received strobe signal has an arbitrary phase relationship with the internal clock signal; and

first and second write blocks to latch the first and second received data signals synchronously with the first and second received strobe signals, respectively.

2. The chip of claim 1, wherein the chip includes data paths, and the data paths that include the first write block are low latency data paths, and the data paths that include the second write block are arbitrary latency data paths.

3. The chip of claim 2, further comprising:

a memory array;

a first read block to be clocked by the internal clock, wherein the first read block interfaces between the first write block and the memory array, and interfaces between the memory array and a transmitter of the second port; and

a second read block to be clocked by the internal clock, wherein the second read block interfaces between the second write block and the memory array, and interfaces between the memory array and a transmitter of the first port.

4. The chip of claim 3, wherein the internal clock signal clocks data in the first and second read clocks at a double data rate.

5. The chip of claim 3, wherein the data paths that include the first read block or that carry data from the memory array to the second port through the second read block are low latency data paths.

6. The chip of claim 1, wherein the internal clock signal is a phase adjusted internal clock signal and wherein the circuitry to provide the internal clock includes delayed locked loop

circuitry that receives a non-phase adjusted internal clock and provides timing signals to an interpolator which produces the phase adjusted internal clock signal.

7. The chip of claim 6, wherein the interpolator receives at least a portion of the phase adjusted internal clock signal as an input and receives a delayed received strobe signal as an input.

8. The chip of claim 6, wherein the internal clock signal is a phase adjusted differential internal clock signal.

9. The chip of claim 1, where in chip repeats data it receives from the first port to a transmitter at the second port.

10. A system comprising:

a first chip and a second chip; and

a third chip comprising:

a first port coupled to first chip to provide a first received data signal and a first received strobe signal;

a second port coupled to second chip to provide a second received data signal and a second received strobe signal;

circuitry to provide an internal clock signal with a fixed phase relationship to the first received strobe signal, wherein the second received strobe signal has an arbitrary phase relationship with the internal clock signal; and

first and second write blocks to latch the first and second received data signals synchronously with the first and second received strobe signals, respectively.

11. The system of claim 10, wherein the third chip repeats data that it receives from the first port to the second chip and data that it receives from the second port to the first chip.

12. The system of claim 10, wherein the third chip includes data paths, and the data paths that include the first write block are low latency data paths, and the data paths that include the second write block are arbitrary latency data paths.

13. The system of claim 12, wherein the third chip further comprises:

a memory array;

a first read block to be clocked by the internal clock, wherein the first read block interfaces between the first write block and the memory array, and interfaces between the memory array and a transmitter of the second port; and

a second read block to be clocked by the internal clock, wherein the second read block interfaces between the second write block and the memory array, and interfaces between the memory array and a transmitter of the first port.

14. The system of claim 13, wherein the internal clock signal clocks data in the first and second read clocks at a double data rate.

15. The system of claim 13, wherein the data paths that include the first read block or that carry data from the memory array to the second port through the second read block are low latency data paths.

16. The system of claim 10, wherein the internal clock signal is a phase adjusted internal clock signal and wherein the circuitry to provide the internal clock includes delayed locked loop circuitry that receives a non-phase adjusted internal clock and provides timing signals to an interpolator which produces the phase adjusted internal clock signal.

17. The system of claim 16, wherein the interpolator receives at least a portion of the phase adjusted internal clock signal as an input and receives a delayed received strobe signal as an input.

18. The system of claim 10, wherein the signaling between the first and second chips and between the second and third chips is simultaneous bi-directional and the first received data signal and the first received strobe signal are provided responsive to a data signal and a strobe signal from the first chip, and the second received data signal and the second received strobe signal are provided responsive to a data signal and a strobe signal from the second chip.

19. A chip comprising:

a first port to provide a first received data signal and a first received strobe signal;

a second port to provide a second received data signal and a second received strobe signal;

circuitry to provide a phase adjusted internal clock signal with a fixed phase relationship to the first received strobe signal, wherein the second received strobe signal has an arbitrary phase relationship with the internal clock signal; and

delay circuitry to delay the first received data strobe signal to latch the first data and to delay the second received data strobe signal to latch the second received data signal.

20. The chip of claim 19, wherein the chip includes data paths, and the data paths that include the first write block are low latency data paths, and the data paths that include the second write block are arbitrary latency data paths.

21. The chip of claim 20, further comprising:

a memory array;

a first read block to be clocked by the internal clock, wherein the first read block interfaces between the first write block and the memory array, and interfaces between the memory array and a transmitter of the second port; and

a second read block to be clocked by the internal clock, wherein the second read block interfaces between the second write block and the memory array, and interfaces between the memory array and a transmitter of the first port.